For publication in Electronics magazine

12 Pp

A LOW-POWER ANALOG-TO-DIGITAL CONVERTER

By Thomas B. Fryer and Charles W. Beck

Instrumentation Division, NASA
Ames Research Center, Moffett Field, California

12 PAGES

SUMMARY

An accurate, low-power, analog-to-digital converter has been designed for use in a space vehicle experiment. Since analog-to-digital converters are required in many other applications, the circuit described is considered to be of more general interest than the particular use described. The readout is eight-bit binary with stages interconnected to give serial shift-register output as well as parallel output. The system should be useful for any application requiring a miniature, low-power, digital voltage readout.

INTRODUCTION

The circuit to be described is the analog-to-digital converter and shift-register portion of a complete space experiment package. A brief description of the experiment is of value in understanding the requirements to be met by the A-D converter design and how the general-purpose design resulted.

The experiment was designed for use on the S-57 Orbiting Solar Observatory to measure the Earth-Albedo (reflected light from the Earth and its atmosphere) from an altitude of approximately 500 miles. The

data system on the vehicle required information encoded in an eight-bit binary code and a shift-register output upon command from the telemetry system. The measured data consisted of analog readings from six photomultiplier tubes with optical filters to cover various spectral bands from 3000 Å to 9000 Å. These outputs were commutated with a solid-state switch and amplified to a 0-5 volt low-impedance analog output. This signal was then processed in the A-D converter. The remainder of the instrument had low-voltage power supplies, a high-voltage photomultiplier supply, and a logic circuitry for proper data readin and readout sequencing in relation to the vehicle spin and telemetry system.

A number of types of A-D converters were considered in order to achieve the experimental requirements. The system to be described was selected because its accuracy is dependent only upon the on-off switching of a matrix of precision resistors and a regulated d-c power supply. The active components merely serve a logic on-off function or provide gain that is stabilized with feedback. The system selected also has the additional advantage that the conversion process may be made continuous; hence, the converter can track input data within its frequency response limitations. This allows a sample and hold operation for accurate readin and readout at any selected instant of time.

PRINCIPLE OF OPERATION

Figure 1 is a block diagram of the A-D converter. The converter consists basically of eight bistable multivibrators interconnected as

an up-down counter and driven by a multivibrator clock. The binaries control a digital-to-analog converter connected to the summing junction of a high-gain operational-type amplifier. The analog input is also connected to the summing junction through a suitable summing resistor, and is of opposite polarity to the current from the digital-to-analog matrix. The summing amplifier then controls the gates which determine whether an up or down count is required of the binary in order to reach a null.

Counter Circuit

The operation of the eight-bit binary counter is best understood by examining the gating connections shown with the typical binary, figure 2. Connection 6 is the conventional toggle connection and if the trigger input is derived from the right side of the previous binary in the chain (connection 5), the counter chain will logically count forward or, in other words, scale up. If, however, the trigger is obtained from the left side (connection 4), a down count results. Thus a second toggle (connection 7) is tied to connection 4 of the previous binary. The up-scale and down-scale gates that are tied to connections 8 and 9, respectively, determine which toggle is in operation. The other binary connections are the 6-volt power supply, the ground, and connection 1 that is used for shift-control operation.

The up- and down-scale gates are driven so that one is "on" and the other "off" at any instant of time; therefore scaling will take place either up or down, depending upon the output of the error amplifier as

the clock pulses feed into the first binary (B_0). A second logic connection to the up- and down-scale gates is from the count controls. Two transistors with appropriate diodes to the various binaries provide an up and down limit control. When the binaries reach any prescribed count for which the up-limiter is set, the up gate is inhibited and only a down-count operation is possible. The down limit control works in a similar manner. In this particular application the up limit is set at 255 and the down limit is set at 15. A third connection is from the digitize signal. Thus, for the counter to scale, the error-amplifier signal must be present, the counter must not be at the limit in the direction of count, and the external digitize command must be present.

The application of a pulse to the shift line (tied to connection 1 of all binaries) transfers the condition of B_{n-1} to B_n, etc., by means of the diode gating to the bases of the binary transistors. Of course, it is necessary when shift pulses are applied to inhibit both the up-down gates by the absence of the digitize commands. Control of the shift and digitizing command is accomplished in a logic circuit external to the circuit shown. The timing of these pulses allows the circuit to digitize and readout upon command. During the shifting operation, eight pulses are applied to the shift line in order to read the "0" or "1" conditions of all the binaries. The shift operation is also nondestructive since connections 2 and 3 of the first binary are tied to connections 4 and 5 of the last binary to provide an end-around carry. This then returns the entire system to the same condition after eight pulses that existed prior to the shift operation. This feature speeds up the

digitizing operation since the count is not reset after each readout and the scaler only has to take care of any incremental change that occurred during the shifting operation.

Digital-to-Analog Converter

The key element in the type of A-D converter being described is the D-A conversion. At first glance the need for a D-A converter may seem a devious way to get an A-D converter, but the simplicity and accuracy of a D-A converter (merely a set of weighted resistors) are the advantages of this approach. In effect, the use of a D-A converter as a feedback element in the system provides its inverse function or, in other words, A-D conversion. A matrix of appropriate weighted precision resistors is connected to the binaries, each of which, of course, can only have two conditions, 0 volts or B+ corresponding to the binary states "0" and "1." When the correct balancing current at the summing node of the error amplifier is accomplished, all the binaries will be at their proper "0" or "1" conditions representative of the analog input voltage. When current balance equivalent to less than one count is accomplished up-down scaling stops until the input changes and causes an unbalance which then requires a new unique binary condition.

The system accuracy depends entirely upon the accuracy of the components at the summing junction, and since these consist of selected precision resistors and not active components, great accuracy is possible. A series of three resistors is used from each of the first four binaries to avoid high resistance values that were not available in the small

packages required. The use of the resistor networks and lower resistance values provides more rapid null balancing since capacity effects are reduced.

Precision transistor switches were not necessary in the circuit to drive the D-A converter since the saturation voltage of the binaries was sufficiently stable. Since this saturation voltage is not zero, however, some zero offset adjustment is provided at the input to the summing amplifier. The demand for a system with more than eight-bits accuracy, however, would probably require the use of saturated transistor switches. The over-all accuracy would be limited only by resistor precision, power supply accuracy, offset errors in the transistor switches, and drift in the error amplifier. The use of 13 bits and 0.01% accuracy would appear to be entirely practical with proper selection of these critical items.

Error Amplifier

The error amplifier is a solid-state, low-level analog amplifier. The use of the 2N2484 transistors with a typical β of 250 at an I_c of 10μa reduces the input current and, hence, any consequent errors to a very low value. The 2N2484 can be obtained as a matched pair in one envelope which will minimize voltage drift due to temperature gradients. The use of individual transistors, however, gave errors of less than 3 millivolts over a temperature of 0° to 50° C and therefore was more than adequate for the eight-bit (1 part in 256) system used. The open-loop amplifier gain is greater than 2000.

Feedback is provided in the error amplifier to stabilize the overall gain to about 300. This gain is just sufficient to operate the appropriate up- or down-gate when the error at the summing junction exceeds the equivalent of ±1/2 count. The use of a stabilized gain prevents the circuit from oscillating about a one count error at balance. The error amplifier is followed by a two-transistor inverter circuit to supply balanced drive to the up- and down-count control gates.

CIRCUIT PERFORMANCE

The complete system as shown in the schematic diagram consumes 35 milliwatts of power at null. The error amplifier requires only 6 milliwatts while each of the binaries requires only 3 milliwatts. The use of low-power binaries results in approximately a 30 kilocycles per second frequency limit. The use of more power would allow faster digitizing speed by the use of a higher-frequency clock. With the 20 kilocycle clock used, the time required to slew from a zero null to full scale is 12.5 milliseconds. The summing resistors used with the error amplifier provided an analog-input resistance of 10K ohms per volt. Thermal drift was less than one count over a temperature range of -10° to $+60^{\circ}$ C.

CONCLUDING REMARKS

The A-D converter described should be very useful for any application requiring a miniature, low-power, digital voltage readout. The circuit as shown was designed for a specific application that required low power and only eight-bit accuracy and therefore various compromises were made in the design. The basic system, though, could be applied in

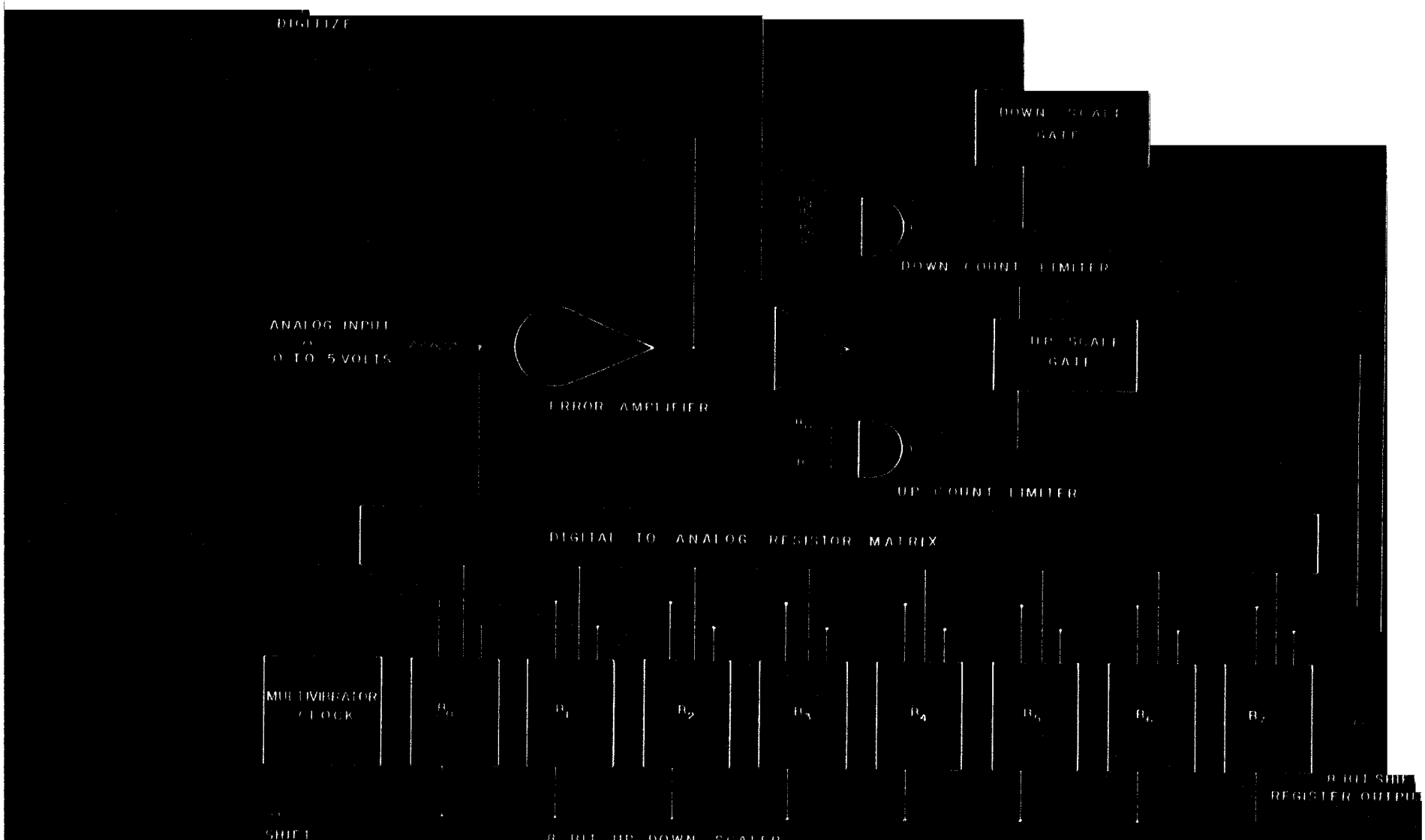
situations requiring a great deal more speed and accuracy by using more binaries and saturated switches, with correspondingly greater power consumption.

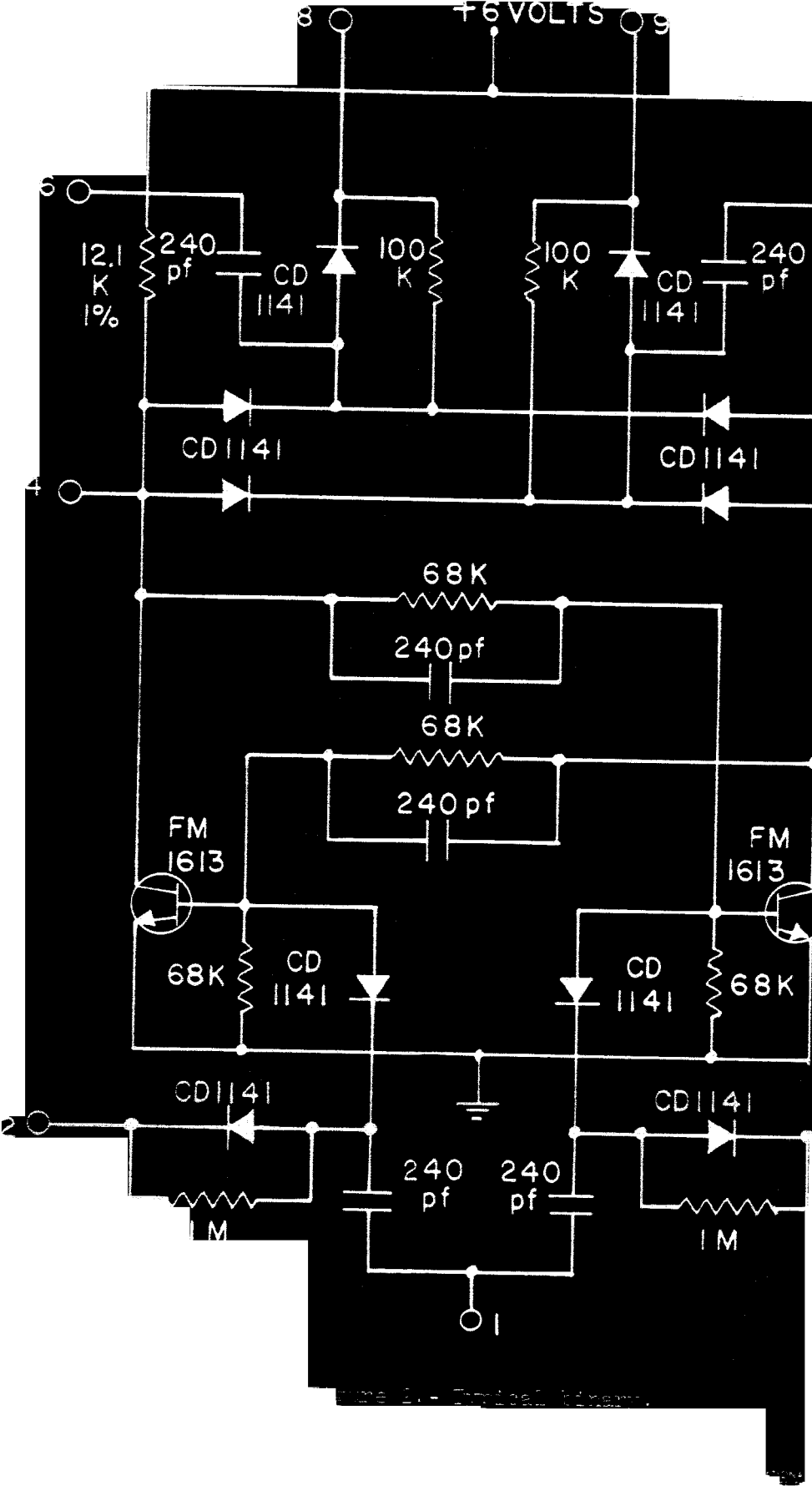
The circuit is, in effect, a solid-state servo with all the characteristics of an electromechanical servo but without moving parts. Its slewing rate is limited by the clock and is thus similar to the maximum slewing rate of a mechanical servo, but of course much greater speed is possible with the electronic circuit. Upper and lower limit stops are possible. Continuous conversion is obtained with very accurate operation similar to an electromechanical servo. The system could be considered for servo application, where a combination of medium speed and accuracy is required.

FIGURE TITLES

Figure 1.- Block diagram of the A-D converter.

Figure 2.- Typical binary.


DIGITIZE
DOWN SCALE GATE
DOWN COUNT LIMITER
ANALOG INPUT
0 TO 5 VOLTS
ERROR AMPLIFIER
UP SCALE GATE
UP COUNT LIMITER
DIGITAL TO ANALOG RESISTOR MATRIX
MULTIVIBRATOR CLOCK
R_0
R_1
R_2
R_3
R_4
R_5
R_6
R_7
REGISTER OUTPUT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9
6
12.1 K 1%
240 pf
CD 1141
100 K
100 K
CD 1141
240 pf
CD1141
CD1141
4
68K
240pf
68K
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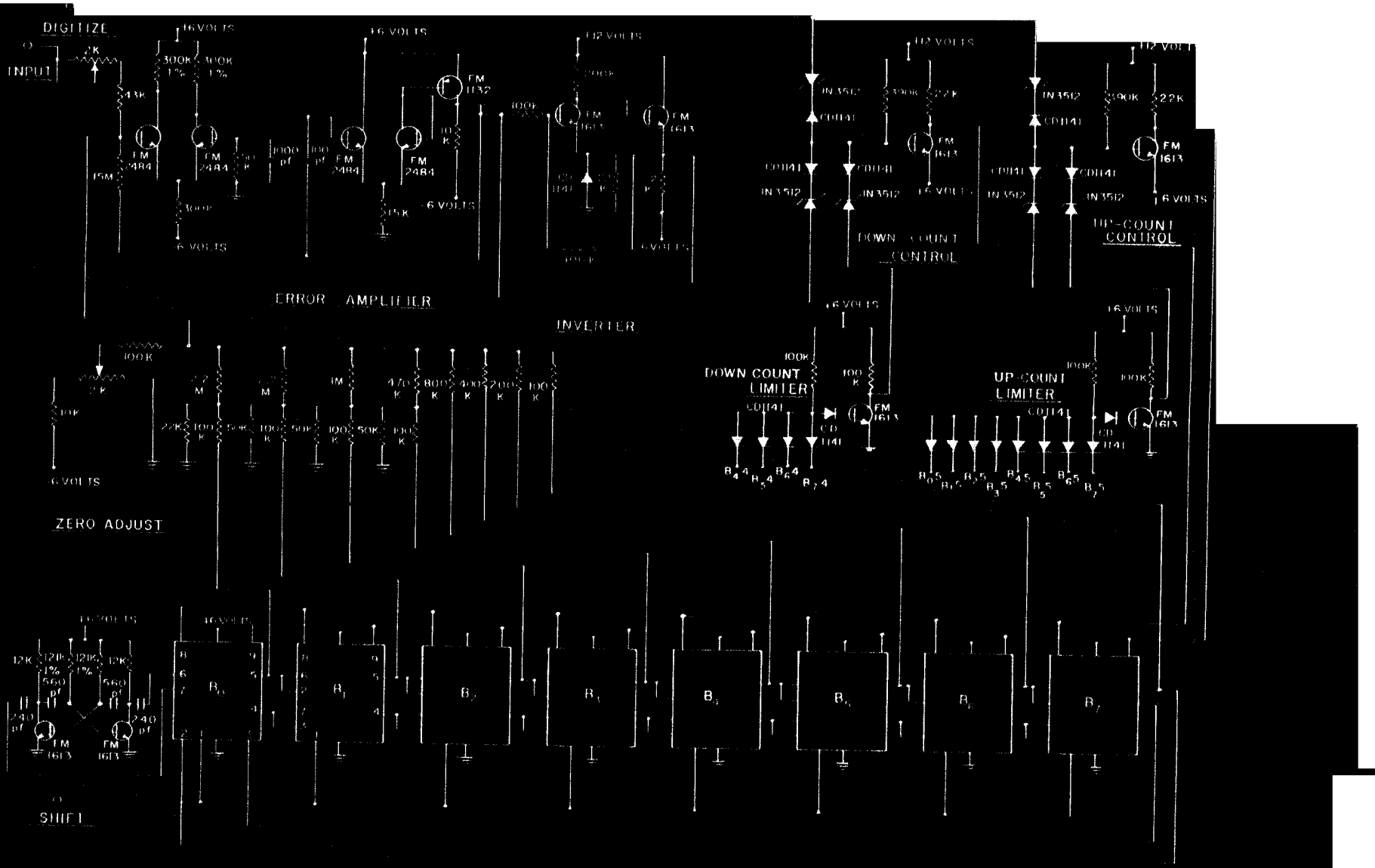

Figure 5. Circuit diagram.